CL74LVC2G06 Dual Inverter Buffer and Driver With Open-Drain Output

General Description

This dual inverter buffer and driver is designed for 1.65-V to5.5-V V_{CC} operation.

The output of the CL74LVC2G06 device is an open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32mA

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Ordering Information

Part Number	Package	
CL74LVC2G06	SOT-23-6 SOT-25 SOT-353 SOT-553	

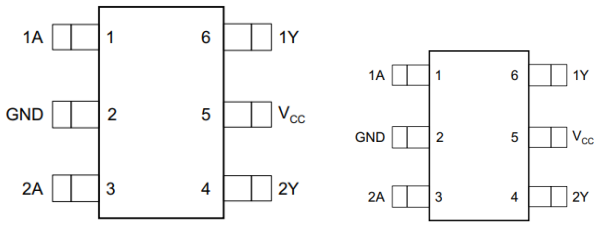
Features

- Supports 5-V V_{CC} Operation
- Max Tpd of 3.4 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V for open-drain devices
- Typical V_{OLP}(Output Ground Bounce)<0.8V at Vcc = 3.3V, T_A= 25℃
- Typical VOHV(Output VOH Undershoot)>2V at Vcc= 3.3V, T_A=25
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5V
- I_{OFF} Supports Live Insertion, Partial-Power-Down Mode and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Supports Down-Translation(5V to 3.3V and 3.3V to 1.8V)
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

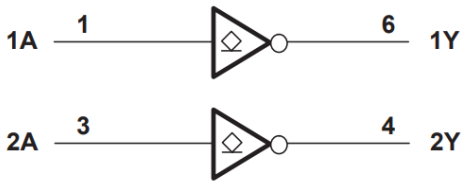
Applications

- AV Receiver
- Blu-ray Player and Home Theater
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PC
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
GND	2	Ground
1A	1	Input 1
2A	3	Input 2
1Y	6	Open-drain output 1
2Y	4	Open-drain output 2
Vcc	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ---------- -0.5V to +6.5V
- V_I ---------- -0.5V to +6.5V
- V_O (Voltage applied to any output in the high-impedance or power-off state) ---------- -0.5V to +6.5V
- V_O (Voltage applied to any output in the high or slow state) ---------- -0.5V to +6.5V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous output current ---------- ±50mA
- Storage Temperature ---------- –65°C to 150°C

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O		0		5.5	V
High- level input voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}			V
		V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 3V to 3.6V	2			
		V_{CC} = 4.5V to 5.5V	0.7 x V_{CC}			
Low- level input voltage	V_{IL}	V_{CC} = 1.65V to 1.95V			0.35 x V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.8	
		V_{CC} = 4.5V to 5.5V			0.3 x V_{CC}	
Low- level output current	I_{OL}	V_{CC} = 1.65V			4	mA
		V_{CC} = 2.3V			8	
		V_{CC} = 3V			16	
		V_{CC} = 3V			24	
		V_{CC} = 4.5V			32	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V_{CC} = 3.3V±0.3V			10	
		V_{CC} = 5V±0.5V			5	
Operating temperature	T_A		-40		125	℃

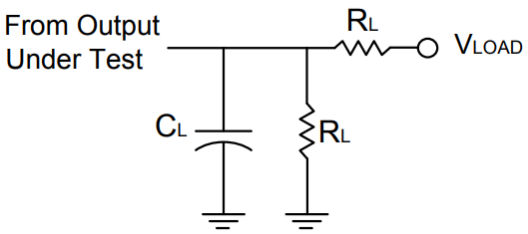
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low- level output voltage	V_{OL}	V_{CC} = 1.65~5.5V, I_{OL}= 100uA			0.1	V
		V_{CC} = 1.65V, I_{OL}= 4mA			0.45	
		V_{CC} = 2.3V, I_{OL}= 8mA			0.3	
		V_{CC} = 3V, I_{OL}= 16mA			0.4	
		V_{CC} = 3V, I_{OL}= 24mA			0.55	
		V_{CC} = 4.5V, I_{OL}= 32mA			0.55	
Inflection-point current	I_I	V_{IN}= 5.5V or GND, V_{CC}= 0~5.5V			±5	uA
Power off leakage current	I_{OFF}	V_I or V_O = 5.5V, V_{CC}=0V			±10	uA
Supply current	I_{CC}	V_I= 5.5V or GND, I_{OUT}=0, V_{CC}=1.65~5.5V			10	uA
Additional supply current per input pin	$\triangle I_{CC}$	V_{CC}=3~5.5V, one input ate V_{CC}-0.6V, other input at V_{CC} or GND			500	uA

Switching Characteristics

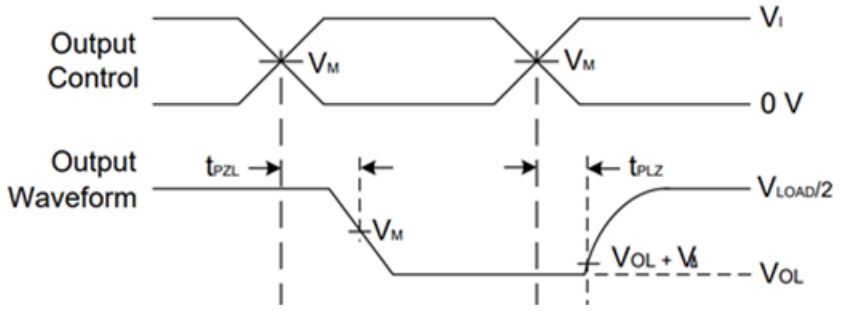
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Propagation delay from input(A) to output(Y)	T_{PD}	V_{CC} = 1.8V±0.15V,	1.8		7.2	ns
		V_{CC} = 2.5V±0.2V	1		3.9	
		V_{CC} = 3.3V±0.3V	1		3.4	
		V_{CC} = 5V±0.5V	1		2.9	

Parameter Measurement Information



TEST	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

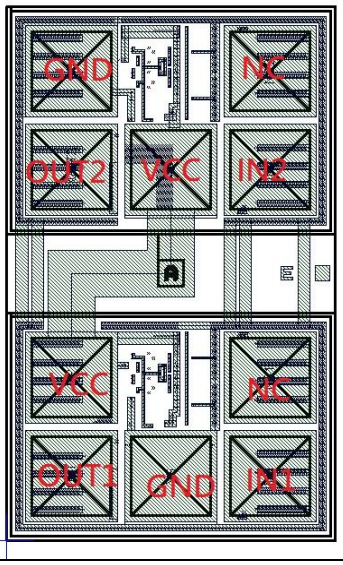
VCC	INPUTS		V_M	V_{LOAD}	C_L	R_L	$V_\triangle$
	V_I	t_r/t_f					
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	2 X V_{CC}	30pF	1kΩ	0.15V
2.5V ± 0.2V	V_{CC}	≦2ns	$V_{CC}/2$	2 X V_{CC}	30pF	500Ω	0.15V
3.3V ± 0.3V	3V	≦2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V ± 0.5V	V_{CC}	≦2.5ns	$V_{CC}/2$	2 X V_{CC}	50pF	500Ω	0.3V



Voltage Waveform Enable and DisableTimes
Low- and High-Level Enabling

Notes:
A. C_L includes probe and jig capacitance
B. All pulses and supplied at pulse repetition rate≦10MHz
C. The Inputs are measured one at a time with one transition per measurement
D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}
E. t_{PZL} is measured at V_M
F. t_{PLZ} is measured at V_{OL} + $V_\triangle$

PAD Location and Coordinates

PHYSICAL CHARACTERISTICS		UNIT	CHIP DRAWING
Wafer Size	200	mm	
Die Size (with S/L)	0.308 * 0.466	mm^2	
Scribe line width	60	um	
TOP Metal thickness	3	µm	
Top Metallization	Al-Cu		
Wafer Thickness	726	µm	
CUP (circuit under PAD) or not	YES		
Bonding Wire Diameter	20	um	

PAD NAME	PAD SIZE (µm²)	Coordinate
IN2	60*60	(199,282)
GND	60*60	(49,357)
GND	60*60	(124,49)
IN1	60*60	(199,49)
OUT1	60*60	(49,49)
VCC	60*60	(49,124)
OUT2	60*60	(49,282)

Bonding Diagram Example