CL74LVC1G240 Single Buffer/Driver With 3-State Output

General Description

This single buffer/driver is designed for 1.65-V to5.5-V VCC operation.

The CL74LVC1G240 device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, OE should be tied to Vcc through a pullup resistor ; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down application using $I_{off.}$ The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CL74LVC1G240 device is available in a variety of packages, including the ultra-small DFN body size of 1 mm × 1 mm.

Ordering Information

Part Number	Package	
CL74LVC1G240	SOT-23-5 SOT-25 SOT-353 SOT-553 DFN1X1-4L	

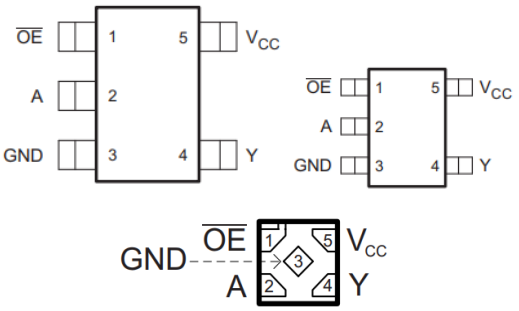
Features

- Available in the Ultra Small DFN1X1
- Supports 5-V Vcc Operation
- Inputs Accept Voltages to 5.5V
- Provides Down Translation to Vcc
- Max Tpd of 3.7 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

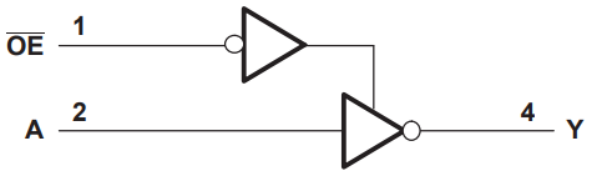
Applications

- Cable Modem Termination System
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Motor Control: High-Voltage
- Power Line Communication Modem
- SSD: Internal or Externa
- Video Broadcasting and Infrastructure: Scalable Platform
- Video Broadcasting: IP-Based Multi-Format Transcoder
- Video Communications System

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
$\overline{OE}$	1	Input
A	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ---------- -0.5V to +6.5V
- V_I ---------- -0.5V to +6.5V
- V_O(Voltage range applied to any output in the high-impedance or power-off state) ---------- -0.5V to V_{CC}+0.5V
- V_O(Voltage range applied to any output in the high or slow state) ---------- -0.5V to V_{CC}+0.5V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous output current ---------- ±50mA
- Storage Temperature ---------- –65°C to 150°C

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O				VCC	V
High- level input voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}			V
		V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 3V to 3.6V	2			
		V_{CC} = 4.5V to 5.5V	0.7 x V_{CC}			
Low- level input voltage	V_{IL}	V_{CC} = 1.65V to 1.95V			0.35 x V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.8	
		V_{CC} = 4.5V to 5.5V			0.3 x V_{CC}	

High- level output current	I_{OH}	V_{CC} = 1.65V			-4	mA
		V_{CC} = 2.3V			-8	
		V_{CC} = 3V			-16	
		V_{CC} = 3V			-24	
		V_{CC} = 4.5V			-32	
Low- level output current	I_{OL}	V_{CC} = 1.65V			4	mA
		V_{CC} = 2.3V			8	
		V_{CC} = 3V			16	
		V_{CC} = 3V			24	
		V_{CC} = 4.5V			32	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V_{CC} = 3.3V±0.3V			10	
		V_{CC} = 5V±0.5V			5	
Operating temperature	T_A		-40		125	℃

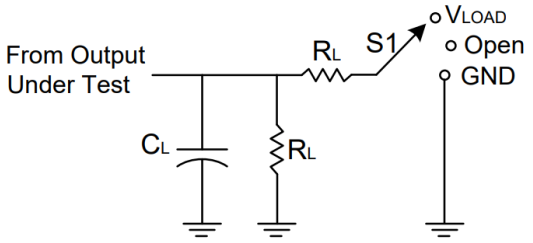
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High- level output voltage	V_{OH}	V_{CC} = 1.65~5.5V, I_{OH}= 100uA	VCC-0.1			V
		V_{CC} = 1.65V, I_{OH}= 4mA	1.2			
		V_{CC} = 2.3V, I_{OH}= 8mA	1.9			
		V_{CC} = 3V, I_{OH}= 16mA	2.4			
		V_{CC} = 3V, I_{OH}= 24mA	2.3			
		V_{CC} = 4.5V, I_{OH}= 32mA	3.8			
Low- level output voltage	V_{OL}	V_{CC} = 1.65~5.5V, I_{OL}= 100uA			0.1	V
		V_{CC} = 1.65V, I_{OL}= 4mA			0.45	
		V_{CC} = 2.3V, I_{OL}= 8mA			0.3	
		V_{CC} = 3V, I_{OL}= 16mA			0.4	
		V_{CC} = 3V, I_{OL}= 24mA			0.55	
		V_{CC} = 4.5V, I_{OL}= 32mA			0.55	
Input leakage current	I_I	V_{IN}= 5.5V or GND, V_{CC}= 0~5.5V			±5	uA
Power off leakage current	I_{OFF}	V_{IN} or V_O= 5.5V, V_{CC}=0V			±10	uA
Quiescent supply current	I_Q	V_{IN}= V_{CC} or GND, I_{OUT}=0, V_{CC}=1.65~5.5V			10	uA
Additional quiescent supply current per input pin	$\triangle I_Q$	V_{CC}=3~5.5V, one input ate V_{CC}-0.6V, other input at V_{CC} or GND			500	uA

Switching Characteristics

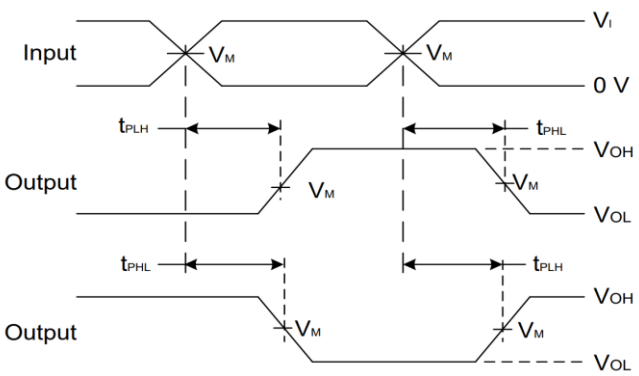
Parameter	From Input	To Output	Test Conditions	Min	Typ	Max	Units
T_{PD}	A	Y	V_{CC} = 1.8V±0.15V	2.8		9	ns
			V_{CC} = 2.5V±0.2V	1.2		5.5	
			V_{CC} = 3.3V±0.3V	1		4.5	
			V_{CC} = 5V±0.5V	1		4	
T_{en}	$\overline{OE}$	Y	V_{CC} = 1.8V±0.15V	3.3		10.1	ns
			V_{CC} = 2.5V±0.2V	1.5		6.6	
			V_{CC} = 3.3V±0.3V	1		5.3	
			V_{CC} = 5V±0.5V	1		5	
T_{dis}	$\overline{OE}$	Y	V_{CC} = 1.8V±0.15V	1.3		9.2	ns
			V_{CC} = 2.5V±0.2V	1		5	
			V_{CC} = 3.3V±0.3V	1		5	
			V_{CC} = 5V±0.5V	1		4.2	

Parameter Measurement Information

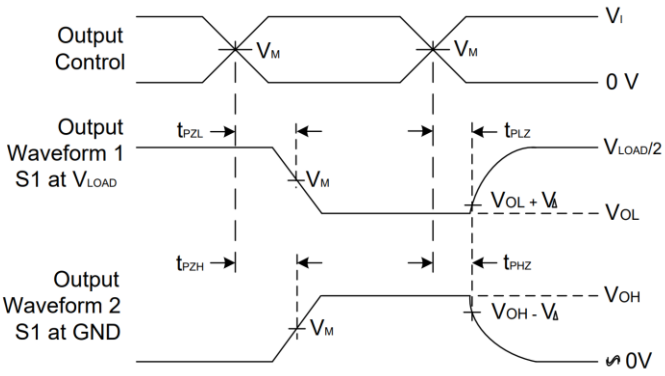


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

VCC	INPUTS		V_M	V_{LOAD}	C_L	R_L	$V\triangle$
	V_I	t_r/t_f					
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	2 X V_{CC}	30pF	1kΩ	0.15V
2.5V ± 0.2V	V_{CC}	≦2ns	$V_{CC}/2$	2 X V_{CC}	30pF	500Ω	0.15V
3.3V ± 0.3V	3V	≦2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V ± 0.5V	V_{CC}	≦2.5ns	$V_{CC}/2$	2 X V_{CC}	50pF	500Ω	0.3V



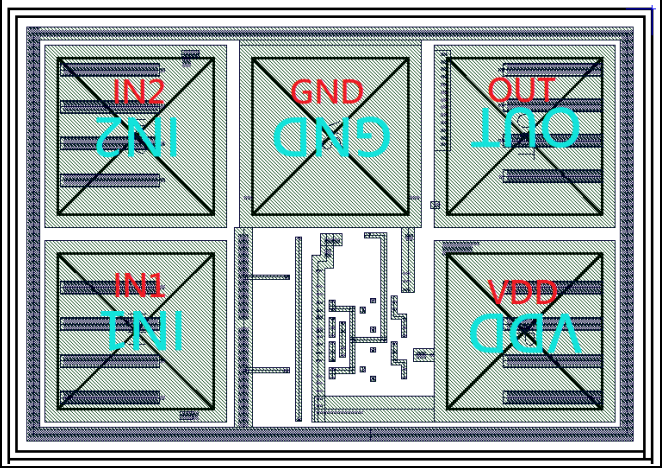
Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs



Voltage Waveform Enable and DisableTimes
Low- and High-Level Enabling

Notes:
A. C_L includes probe and jig capacitance
B. All pulses and supplied at pulse repetition rate≦10MHz
C. The Inputs are measured separately one transition per measurement
D. t_{PLZ} and t_{PHZ} are the same as t_{dis}
E. t_{PZL} and t_{PZH} are the same as t_{en}
F. t_{PLH} and t_{PHL} are the same as t_{PD}

PAD Location and Coordinates

PHYSICAL CHARACTERISTICS		UNIT	CHIP DRAWING
Wafer Size	200	mm	
Die Size (with S/L)	0.308 * 0.233	mm^2	
Scribe line width	60	um	
TOP Metal thickness	3	µm	
Top Metallization	Al-Cu		
Wafer Thickness	726	µm	
CUP (circuit under PAD) or not	YES		
Bonding Wire Diameter	20	um	

PAD NAME	PAD SIZE (µm²)	Coordinate
IN 1	60*60	(49,49)
IN 2	60*60	(49,124)
GND	60*60	(124,124)
OUT (Y)	60*60	(199,124)
VDD	60*60	(199,49)

Bonding Diagram Example