

## CL74LVC1G02 Single 2-Input Positive NOR-Gate

### General Description

This single 2-input positive-NOR gate is designed for 1.65-V to 5.5-V VCC operation.

The CL74LVC1G02 performs the Boolean function  $Y = \overline{A + B}$  in positive logic

The CMOS device has high output drive while maintaining low static power dissipation over a broad V<sub>CC</sub> operating range.

The CL74LVC1G02 device is available in a variety of packages, including the ultra-small DFN body size of 1 mm × 1 mm.

### Ordering Information

Part Number	Package	
CL74LVC1G02	SOT-23-5	
	SOT-25	
	SOT-353	
	SOT-553	
	DFN1X1-4L	

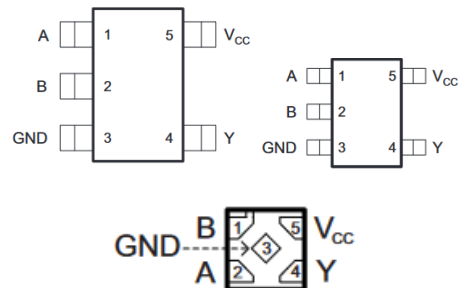
### Features

- Available in the Ultra Small DFN1X1
- Inputs Accept Voltages 1.65V to 5.5 V
- Max Tpd of 3.6 ns at 3.3 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

### Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

### Pin Configuration



### Simplified Schematic



## Pin Assignment

Pin Name	Pin No.	Pin Function
A	1	Input
B	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power pin

## Absolute Maximum Ratings (Note1)

- $V_{CC}$  ----- -0.5V to +6.5V
- $V_I$ ----- -0.5V to +6.5V
- $V_O$ (Voltage range applied to any output in the high-impedance or power-off state)----- -0.5V to +6.5V
- $V_O$ (Voltage range applied to any output in the high or slow state)----- -0.5V to  $V_{CC}+0.5V$
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous clamp current -----  $\pm 50mA$
- Storage Temperature -----  $-65^{\circ}C$  to  $150^{\circ}C$

## Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	$V_{CC}$	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	$V_I$		0		5.5	V
Output voltage	$V_O$				$V_{CC}$	V
High- level input voltage	$V_{IH}$	$V_{CC} = 1.65V$ to $1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC} = 2.3V$ to $2.7V$	1.7			
		$V_{CC} = 3V$ to $3.6V$	2			
		$V_{CC} = 4.5V$ to $5.5V$	$0.7 \times V_{CC}$			
Low- level input voltage	$V_{IL}$	$V_{CC} = 1.65V$ to $1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 3V$ to $3.6V$			0.8	
		$V_{CC} = 4.5V$ to $5.5V$			$0.3 \times V_{CC}$	

High- level output current	$I_{OH}$	$V_{CC} = 1.65V$			-4	mA
		$V_{CC} = 2.3V$			-8	
		$V_{CC} = 3V$			-16	
		$V_{CC} = 3V$			-24	
		$V_{CC} = 4.5V$			-32	
Low- level output current	$I_{OL}$	$V_{CC} = 1.65V$			4	mA
		$V_{CC} = 2.3V$			8	
		$V_{CC} = 3V$			16	
		$V_{CC} = 3V$			24	
		$V_{CC} = 4.5V$			32	
Input transition rise or fall rate	$\Delta T/\Delta V$	$V_{CC} = 1.8V \pm 0.15V, 2.5V \pm 0.2V$			20	ns/V
		$V_{CC} = 3.3V \pm 0.3V$			10	
		$V_{CC} = 5V \pm 0.5V$			5	
Operating temperature	$T_A$		-40		125	$^{\circ}C$

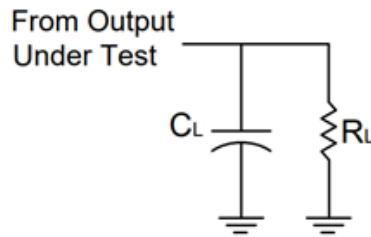
## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High- level output voltage	$V_{OH}$	$V_{CC} = 1.65 \sim 5.5V, I_{OH} = -100\mu A$	$V_{CC} - 0.1$			V
		$V_{CC} = 1.65V, I_{OH} = -4mA$	1.2			
		$V_{CC} = 2.3V, I_{OH} = -8mA$	1.9			
		$V_{CC} = 3V, I_{OH} = -16mA$	2.4			
		$V_{CC} = 3V, I_{OH} = -24mA$	2.3			
		$V_{CC} = 4.5V, I_{OH} = -32mA$	3.8			
Low- level output voltage	$V_{OL}$	$V_{CC} = 1.65 \sim 5.5V, I_{OL} = 100\mu A$			0.1	V
		$V_{CC} = 1.65V, I_{OL} = 4mA$			0.45	
		$V_{CC} = 2.3V, I_{OL} = 8mA$			0.3	
		$V_{CC} = 3V, I_{OL} = 16mA$			0.4	
		$V_{CC} = 3V, I_{OL} = 24mA$			0.55	
		$V_{CC} = 4.5V, I_{OL} = 32mA$			0.55	
Input leakage current	$I_I$	$V_{IN} = 5.5V$ or GND, $V_{CC} = 0 \sim 5.5V$			$\pm 5$	$\mu A$
Power off leakage current	$I_{OFF}$	$V_{IN}$ or $V_O = 5.5V, V_{CC} = 0V$			$\pm 10$	$\mu A$
Supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0, V_{CC} = 1.65 \sim 5.5V$			10	$\mu A$
Additional supply current per input pin	$\Delta I_{CC}$	$V_{CC} = 3 \sim 5.5V$ , one input at $V_{CC} - 0.6V$ , other input at $V_{CC}$ or GND			500	$\mu A$

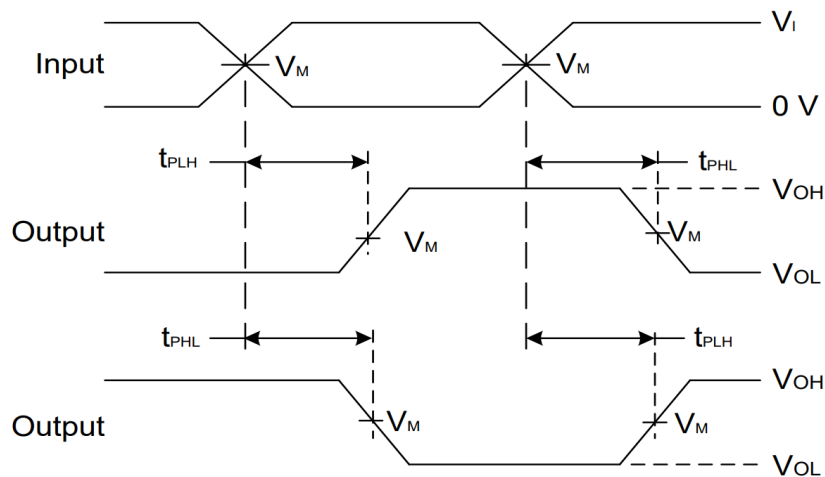
## Switching Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Propagation delay from input(A or B) to output(Y)	$T_{PD}$	$V_{CC} = 1.8V \pm 0.15V,$	$C_L = 15pF$ $R_L = 1M\Omega$			ns
		$V_{CC} = 2.5V \pm 0.2V$				
		$V_{CC} = 3.3V \pm 0.3V$				
		$V_{CC} = 5V \pm 0.5V$				

## Parameter Measurement Information



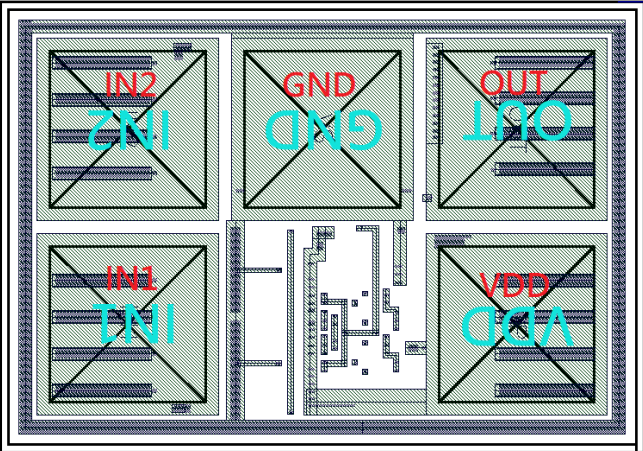
VCC	INPUTS		V <sub>M</sub>	C <sub>L</sub>	R <sub>L</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>			
1.8V ± 0.15V	V <sub>CC</sub>	≤ 2ns	V <sub>CC</sub> /2	15pF	1MΩ
2.5V ± 0.2V	V <sub>CC</sub>	≤ 2ns	V <sub>CC</sub> /2	15pF	1MΩ
3.3V ± 0.3V	3V	≤ 2.5ns	1.5V	15pF	1MΩ
5V ± 0.5V	V <sub>CC</sub>	≤ 2.5ns	V <sub>CC</sub> /2	15pF	1MΩ



**Voltage Waveform Propagation Delay Times  
Inverting and Non Inverting Outputs**

- Notes:
- A. C<sub>L</sub> includes probe and jig capacitance
  - B. All pulses and supplied at pulse repetition rate ≤ 10MHz
  - C. The Inputs are measured separately one transition per measurement
  - D. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>PD</sub>

## PAD Location and Coordinates

PHYSICAL CHARACTERISTICS		UNIT	CHIP DRAWING
Wafer Size	200	mm	
Die Size (with S/L)	0.308 * 0.233	mm <sup>2</sup>	
Scribe line width	60	um	
TOP Metal thickness	3	um	
Top Metallization	Al-Cu		
Wafer Thickness	726	um	
CUP (circuit under PAD) or not	YES		
Bonding Wire Diameter	20	um	

PAD NAME	PAD SIZE (μm <sup>2</sup> )	Coordinate
IN 1	60*60	(49,49)
IN 2	60*60	(49,124)
GND	60*60	(124,124)
OUT (Y)	60*60	(199,124)
VDD	60*60	(199,49)

Bonding Diagram Example

