# CL74AUP1G125 Low-Power Single Bus Buffer Gate With 3-State Output

## General Description

The bus buffer gate is designed for 0.8-V to 3.6-V VCC operation.

The CL74AUP1G125 device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CL74AUP1G125 device is available in a variety of packages, including the ultra-small DFN body size of 1 mm × 1 mm.

## Ordering Information

| Part Number | Package | |
|---|---|---|
| CL74AUP1G125 | SOT-23-5<br>SOT-25<br>SOT-353<br>SOT-553<br>DFN1X1-4L | |

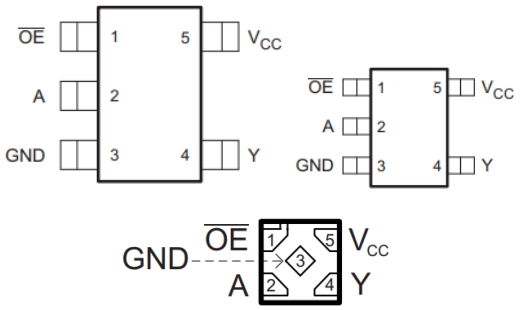
## Features

- Available in the Ultra Small DFN1X1
- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 4.7 ns at 3.3 V
- Low Static-Consumption, 0.9-μA Max $I_{CC}$
- Low Noise Overshoot and Undershoot<10% of $V_{CC}$
- Input-Disable Feature Allows Floating Input Conditions
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input($V_{hys}$= 250mV Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

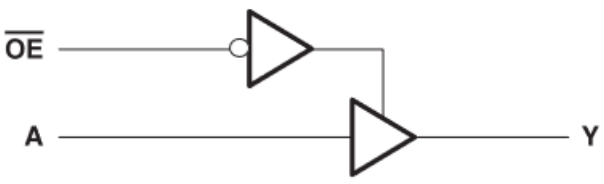
## Applications

- Audio Dock: Portable
- BluRay™ Players and Home Theaters
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Wireless Headsets, Keyboards and Mice

## Pin Configuration




## Simplified Schematic



## Pin Assignment

| Pin Name | Pin No. | Pin Function |
|---|---|---|
| $\overline{OE}$ | 1 | Input |
| A | 2 | Input |
| GND | 3 | Ground |
| Y | 4 | Output |
| VCC | 5 | Power pin |

## Absolute Maximum Ratings (Note1)

- $V_{CC}$ ---------- -0.5V to +4.6V
- $V_I$ ---------- -0.5V to +4.6V
- $V_O$(Voltage range applied to any output in the high-impedance or power-off state) ---------- -0.3V to $V_{CC}$+0.3V
- $V_O$(Voltage range applied to any output in the high or slow state) ---------- -0.3V to $V_{CC}$+0.3V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous output current ---------- ±20mA
- Storage Temperature ---------- –65°C to 150°C

## Recommended Operating Conditions

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | Operating | 0.8 | | 3.6 | V |
| Input voltage | $V_I$ | | 0 | | 3.6 | V |
| Output voltage | $V_O$ | | 0 | | VCC | V |
| High- level input voltage | $V_{IH}$ | $V_{CC}$ = 0.8V | $V_{CC}$ | | | V |
| | | $V_{CC}$ = 1.1V to 1.95V | 0.65 x$V_{CC}$ | | | |
| | | $V_{CC}$ = 2.3V to 2.7V | 1.6 | | | |
| | | $V_{CC}$ = 3V to 3.6V | 2 | | | |
| Low- level input voltage | $V_{IL}$ | $V_{CC}$ = 0.8V | | | 0 | V |
| | | $V_{CC}$ = 1.1V to 1.95V | | | 0.35 x $V_{CC}$ | |
| | | $V_{CC}$ = 2.3V to 2.7V | | | 0.7 | |
| | | $V_{CC}$ = 3V to 3.6V | | | 0.9 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| High- level output current | $I_{OH}$ | $V_{CC}$ = 0.8V | | | -20 | uA |
| | | $V_{CC}$ = 1.1V | | | -1.1 | mA |
| | | $V_{CC}$ = 1.4V | | | -1.7 | |
| | | $V_{CC}$ = 1.65V | | | -1.9 | |
| | | $V_{CC}$ = 2.3V | | | -3.1 | |
| | | $V_{CC}$ = 3V | | | -4 | |
| Low- level output current | $I_{OL}$ | $V_{CC}$ = 0.8V | | | 20 | uA |
| | | $V_{CC}$ = 1.1V | | | 1.1 | mA |
| | | $V_{CC}$ = 1.4V | | | 1.7 | |
| | | $V_{CC}$ = 1.65V | | | 1.9 | |
| | | $V_{CC}$ = 2.3V | | | 3.1 | |
| | | $V_{CC}$ = 3V | | | 4 | |
| Input transition rise or fall rate | △T/△V | $V_{CC}$ = 0.8V to 3.6V | | | 200 | ns/V |
| Operating temperature | $T_A$ | | -40 | | 85 | ℃ |

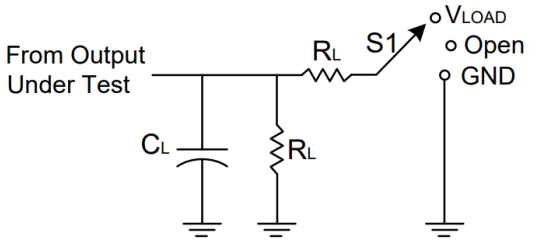
## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High- level output voltage | $V_{OH}$ | $V_{CC}$ = 0.8~3.6V, $I_{OH}$= -20uA | $V_{CC}$-0.1 | | | V |
| | | $V_{CC}$ = 1.1V, $I_{OH}$= -1.1mA | 0.75 x$V_{CC}$ | | | |
| | | $V_{CC}$ = 1.4V, $I_{OH}$= -1.7mA | 1.11 | | | |
| | | $V_{CC}$ = 1.65V, $I_{OH}$= -1.9mA | 1.32 | | | |
| | | $V_{CC}$ = 2.3V, $I_{OH}$= -2.3mA | 2.05 | | | |
| | | $V_{CC}$ = 2.3V, $I_{OH}$= -3.1mA | 1.9 | | | |
| | | $V_{CC}$ = 3V, $I_{OH}$= -2.7mA | 2.72 | | | |
| | | $V_{CC}$ = 3V, $I_{OH}$= -4mA | 2.6 | | | |
| Low- level output voltage | $V_{OL}$ | $V_{CC}$ = 0.8~3.6V, $I_{OL}$= 20uA | | | 0.1 | V |
| | | $V_{CC}$ = 1.1V, $I_{OL}$= 1.1mA | | | 0.3 x$V_{CC}$ | |
| | | $V_{CC}$ = 1.4V, $I_{OL}$= 1.7mA | | | 0.31 | |
| | | $V_{CC}$ = 1.65V, $I_{OL}$= 1.9mA | | | 0.31 | |
| | | $V_{CC}$ = 2.3V, $I_{OL}$= 2.3mA | | | 0.31 | |
| | | $V_{CC}$ = 2.3V, $I_{OL}$= 3.1mA | | | 0.44 | |
| | | $V_{CC}$ = 3V, $I_{OL}$= 2.7mA | | | 0.31 | |
| | | $V_{CC}$ = 3V, $I_{OL}$= 4mA | | | 0.44 | |
| Input leakage current | $I_I$ | $V_{IN}$= 3.6V or GND, $V_{CC}$= 0~3.6V | | | 0.1 | uA |
| Power off leakage current | $I_{OFF}$ | $V_I$ or $V_O$=0V to 3.6V, $V_{CC}$=0V | | | 0.2 | uA |
| Supply current | $I_{CC}$ | $V_I$= GND or ($V_{CC}$ to 3.6V), $I_{OUT}$=0, $V_{CC}$=0.8~3.6V | | | 0.5 | uA |
| Additional supply current per input pin | △$I_{CC}$ | $V_I$= $V_{CC}$-0.6V, $I_{OUT}$=0 | | | 40 | uA |

## Switching Characteristics

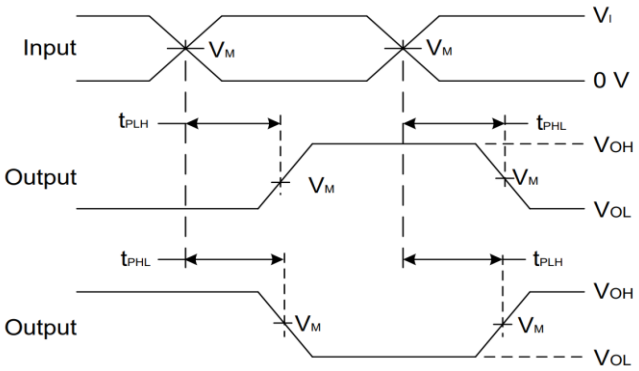
| Parameter | From Input | To Output | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $T_{PD}$ | A | Y | $V_{CC}$ = 0.8V | | 22.5 | | ns |
| | | | $V_{CC}$ = 1.2V±0.1V, | 5.8 | 9.3 | 15.1 | |
| | | | $V_{CC}$ = 1.5V±0.1V, | 4.4 | 6.6 | 10.2 | |
| | | | $V_{CC}$ = 1.8V±0.15V | 3.5 | 5.3 | 8.3 | |
| | | | $V_{CC}$ = 2.5V±0.2V | 2.7 | 3.9 | 5.8 | |
| | | | $V_{CC}$ = 3.3V±0.3V | 2.4 | 3.2 | 4.7 | |
| $T_{en}$ | $\overline{OE}$ | Y | $V_{CC}$ = 0.8V | | 25.2 | | ns |
| | | | $V_{CC}$ = 1.2V±0.1V, | 7 | 11.3 | 18.1 | |
| | | | $V_{CC}$ = 1.5V±0.1V, | 5.5 | 8.1 | 12.2 | |
| | | | $V_{CC}$ = 1.8V±0.15V | 4.3 | 6.5 | 10.1 | |
| | | | $V_{CC}$ = 2.5V±0.2V | 3.4 | 4.8 | 7.1 | |
| | | | $V_{CC}$ = 3.3V±0.3V | 2.9 | 4.1 | 5.9 | |
| $T_{dis}$ | $\overline{OE}$ | Y | $V_{CC}$ = 0.8V | | 14 | | ns |
| | | | $V_{CC}$ = 1.2V±0.1V, | 3.7 | 5.8 | 8.2 | |
| | | | $V_{CC}$ = 1.5V±0.1V, | 5.5 | 3.9 | 5.9 | |
| | | | $V_{CC}$ = 1.8V±0.15V | 3.3 | 4.5 | 6.6 | |
| | | | $V_{CC}$ = 2.5V±0.2V | 2.3 | 3.2 | 4.3 | |
| | | | $V_{CC}$ = 3.3V±0.3V | 2.4 | 4.8 | 6.2 | |

## Parameter Measurement Information

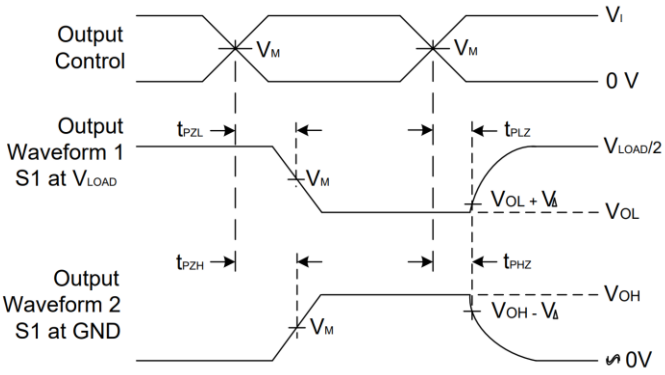



| TEST | S1 | $R_L$ |
|---|---|---|
| $t_{PLH}/t_{PHL}$ | Open | 1MΩ |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ | 5KΩ |
| $t_{PHZ}/t_{PZH}$ | GND | 5KΩ |

| VCC | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | V△ |
|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | |
| 0.8V | $V_{CC}$ | ≦3ns | $V_{CC}/2$ | 2 X $V_{CC}$ | 15pF | 0.1V |
| 1.2V±0.1V, | $V_{CC}$ | ≦3ns | $V_{CC}/2$ | 2 X $V_{CC}$ | 15pF | 0.1V |
| 1.5V±0.1V, | $V_{CC}$ | ≦3ns | $V_{CC}/2$ | 2 X $V_{CC}$ | 15pF | 0.1V |
| 1.8V±0.15V | $V_{CC}$ | ≦3ns | $V_{CC}/2$ | 2 X $V_{CC}$ | 15pF | 0.15V |
| 2.5V±0.2V | $V_{CC}$ | ≦3ns | $V_{CC}/2$ | 2 X $V_{CC}$ | 15pF | 0.15V |
| 3.3V±0.3V | $V_{CC}$ | ≦3ns s | $V_{CC}/2$ | 2 X $V_{CC}$ | 15pF | 0.3V |



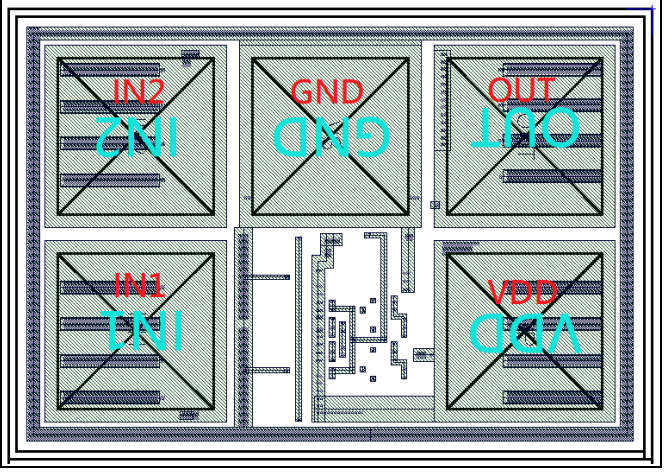

**Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs**




**Voltage Waveform Enable and DisableTimes Low- and High-Level Enabling**

Notes:
A. $C_L$ includes probe and jig capacitance
B. All pulses and supplied at pulse repetition rate≦10MHz
C. The Inputs are measured separately one transition per measurement
D. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$
E. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{PD}$

## PAD Location and Coordinates

| PHYSICAL CHARACTERISTICS | | UNIT | CHIP DRAWING |
|---|---|---|---|
| Wafer Size | 200 | mm |  |
| Die Size (with S/L) | 0.308 * 0.233 | $mm^2$ | |
| Scribe line width | 60 | um | |
| TOP Metal thickness | 3 | µm | |
| Top Metallization | Al-Cu | | |
| Wafer Thickness | 726 | µm | |
| CUP (circuit under PAD) or not | YES | | |
| Bonding Wire Diameter | 20 | um | |



| PAD NAME | PAD SIZE (µm²) | Coordinate |
|---|---|---|
| IN 1 | 60*60 | (49,49) |
| IN 2 | 60*60 | (49,124) |
| GND | 60*60 | (124,124) |
| OUT (Y) | 60*60 | (199,124) |
| VDD | 60*60 | (199,49) |

## Bonding Diagram Example