CL74AUP1G06 Low Power Single Inverter With Open-Drain Outputs

General Description

This single inverter buffer and driver is designed for 0.8-V to 3.6-V V_{CC} operation.

The output of the CL74AUP1G06 device is open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{OFF} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Ordering Information

Part Number	Package	
CL74AUP1G06	SOT-23-5 SOT-25 SOT-353 SOT-553 DFN1X1-4L	

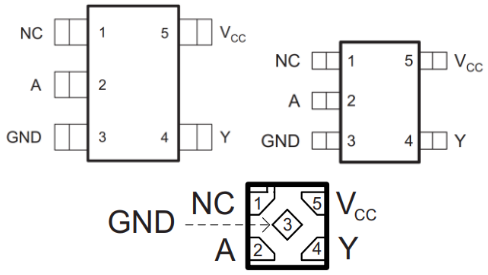
Features

- Available in the Ultra Small DFN1X1
- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 6 ns at 3.3 V
- Low Static-Consumption, 0.9-µA Max I_{CC}
- Low Noise Overshoot and Undershoot<10% of V_{CC}
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input(V_{hys}= 250mV Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

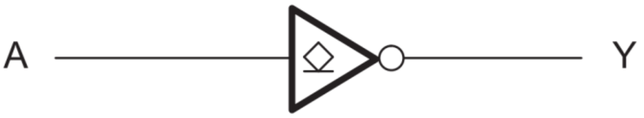
Applications

- AV Receivers
- Smrartphone
- Blu-ray Player and Home Theater
- Desktop or Notebook PCs
- Embedded PC
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablet: Enterprise
- Audio Dock: Portable

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
NC	1	No connect
A	2	Input
GND	3	Ground
Y	4	Output
V_{CC}	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} -- -0.5V to +4.6V
- V_I-- -0.5V to +4.6V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) --------------- -0.3V to +4.6V
- V_O(Voltage range applied to any output in the high or slow state)--------------- -0.3V to V_{CC}+0.3V
- Input clamp current -- -50mA
- Output clamp current --- -50mA
- Continuous clamp current --- ±20mA
- Storage Temperature --- –65°C to 150°C

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	0.8		3.6	V
Input voltage	V_I		0		3.6	V
Output voltage	V_O		0		3.6	V
High- level input voltage	V_{IH}	V_{CC} = 0.8V	V_{CC}			V
		V_{CC} = 1.1V to 1.95V	0.65 xV_{CC}			
		V_{CC} = 2.3V to 2.7V	1.6			
		V_{CC} = 3V to 3.6V	2			
Low- level input voltage	V_{IL}	V_{CC} = 0.8V			0	V
		V_{CC} = 1.1V to 1.95V			0.35 x V_{CC}	
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.9	

Low- level output current	I_{OL}	V_{CC} = 0.8V			20	uA
		V_{CC} = 1.1V			1.1	mA
		V_{CC} = 1.4V			1.7	
		V_{CC} = 1.65V			1.9	
		V_{CC} = 2.3V			3.1	
		V_{CC} = 3V			4	
Input transition rise or fall rate	△T/△V	V_{CC} = 0.8V to 3.6V			200	ns/V
Operating temperature	T_A		-40		85	℃

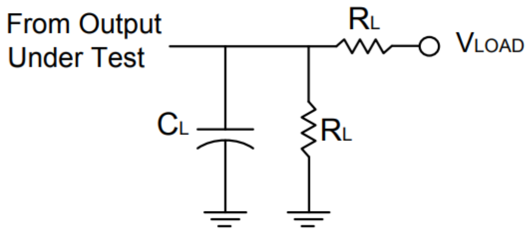
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low- level output voltage	V_{OL}	V_{CC} = 0.8~3.6V, I_{OH}= 20uA			0.1	V
		V_{CC} = 1.1V, I_{OL}= 1.1mA			0.3 xV_{CC}	
		V_{CC} = 1.4V, I_{OL}= 1.7mA			0.31	
		V_{CC} = 1.65V, I_{OL}= 1.9mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 2.3mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 3.1mA			0.44	
		V_{CC} = 3V, I_{OL}= 2.7mA			0.31	
		V_{CC} = 3V, I_{OL}= 4mA			0.44	
Input leakage current	I_I	V_{IN}= 3.6V or GND, V_{CC}= 0~3.6V			0.1	uA
Power off leakage current	I_{OFF}	V_I or V_O=0V to 3.6V, V_{CC}=0V			0.2	uA
Supply current	I_{CC}	V_I= GND or (V_{CC} to 3.6V), I_{OUT}=0, V_{CC}=0.8~3.6V			0.5	uA
Additional supply current per input pin	△I_{CC}	V_I= V_{CC}-0.6V, I_{OUT}=0			40	uA

Switching Characteristics

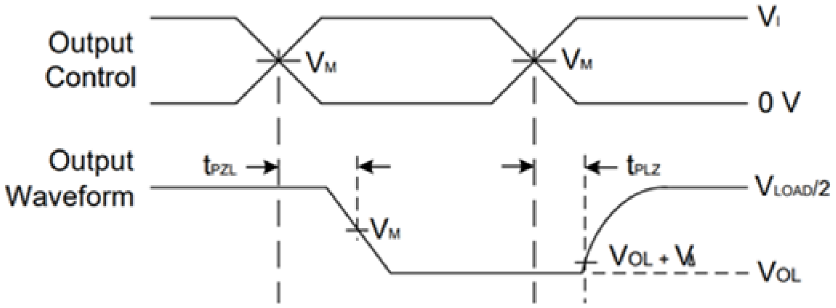
Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Propagation delay from input(A or B) to output(Y)	T_{PD}	V_{CC} = 0.8V	C_L=15pF		17.4		ns
		V_{CC} = 1.2V±0.1V,		4.9	12	12.2	
		V_{CC} = 1.5V±0.1V,		3.5	5	7.7	
		V_{CC} = 1.8V±0.15V		3.2	4.8	6.6	
		V_{CC} = 2.5V±0.2V		2.5	3.5	4.5	
		V_{CC} = 3.3V±0.3V		2	3.8	6	

Parameter Measurement Information



TEST	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

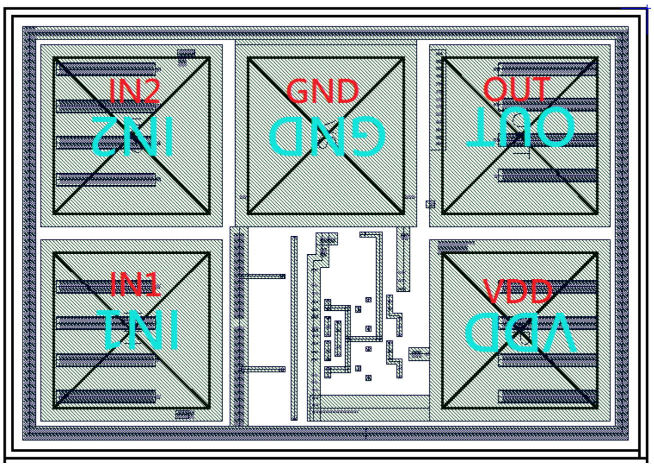
VCC	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
0.8V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
1.2V ± 0.1V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
1.5V ± 0.1V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
2.5V ± 0.2V	3V	≦2.5ns	1.5V	15pF	5KΩ
3.3V ± 0.3V	V_{CC}	≦2.5ns	$V_{CC}/2$	15pF	5KΩ



Voltage Waveform Enable and DisableTimes
Low- and High-Level Enabling

Notes:
A. C_L includes probe and jig capacitance
B. All pulses and supplied at pulse repetition rate ≦10MHz
C. The Inputs are measured one at a time with one transition per measurement
D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}
E. t_{PZL} is measured at V_M
F. t_{PLZ} is measured at $V_{OL} + V_\triangle$

PAD Location and Coordinates

PHYSICAL CHARACTERISTICS		UNIT	CHIP DRAWING
Wafer Size	200	mm	
Die Size (with S/L)	0.308 * 0.233	mm^2	
Scribe line width	60	um	
TOP Metal thickness	3	µm	
Top Metallization	Al-Cu		
Wafer Thickness	726	µm	
CUP (circuit under PAD) or not	YES		
Bonding Wire Diameter	20	um	

PAD NAME	PAD SIZE (μm^2)	Coordinate
IN 1	60*60	(49,49)
IN 2	60*60	(49,124)
GND	60*60	(124,124)
OUT (Y)	60*60	(199,124)
VDD	60*60	(199,49)

Bonding Diagram Example