CR2045

Cost-Effective, 2A Sink/Source Bus Termination Regulator

General Description

The CR2045 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in Double Data Rate (DDR) memory system to comply with the devices requirements. The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 20mV. The output termination voltage can be tightly regulated to track VDDQ / 2 by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The CR2045 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient.

Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shutdown protection.

Ordering Information

Part Number	Marking	Package
CR2045_ES8	2045 YYWW	PSOP-8

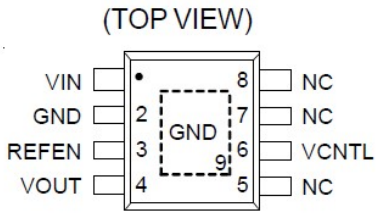
Features

- Ideal for DDR VTT Applications
- Sink and Source Current :
  DDRII 2A Sink/Source @ VIN = 1.8V
  DDRIII 2A Sink/Source @ VIN = 1.5V
  LPDDRIII 2A Sink/Source @ VIN = 1.35V
  DDRIV 2A Sink/Source @ VIN = 1.2V
- Integrated Power MOSFETs
- Generate Termination Voltage for DDR Memory Interfaces
- Stable with Output Ceramic Capacitor
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- RoHS Compliant

Applications

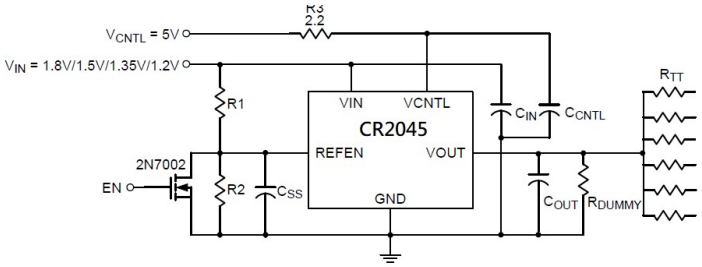
- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR Memory Systems

Pin Configuration



SOP-8 (Exposed Pad)

Typical Application Circuit

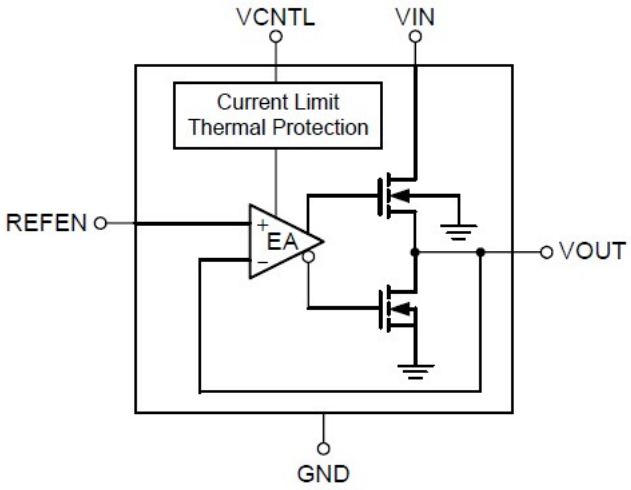


$R_1 = R_2 = 100k\Omega$, $R_{TT} = 50\Omega / 33\Omega / 25\Omega$
$R_{DUMMY} = 1k\Omega$ as for V_{OUT} discharge when V_{IN} is not presented but V_{CNTL} is presented
$C_{OUT} = 10\mu F$ (Ceramic) under the worst case testing condition
$C_{IN} = 10\mu F$, $C_{CNTL} = 1\mu F$, $C_{SS} = 1nF$ to $0.1\mu F$

Pin Assignment

Pin Name	Pin No. PSOP8	Pin Function
VIN	1	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. Large bulk capacitors with low ESR should be placed physically close to this pin to prevent the input rail from dropping during large load transient. A 10uF ceramic capacitor is recommended at this pin. VN I cannot be forced higher than V CNTL otherwise the current limit function may be false triggered and disable the output voltage.
GND	2	**Ground.**
REFEN	3	**Reference Voltage Input.** This pin is the non-inverting input of the error amplifier. The output voltage is regulated to track the reference voltage input. This pin is also monitored by the shutdown comparator. Pulling this pin lower than 0.15V shuts down this device.
VOUT	4	**Output Voltage.** This pin is power output of the device. A pull low resistance exists when the device is disabled by pulling low the EN pin. To maintain adequate transient response to large load change, typical value of 1000uF Al electrolytic capacitor with 10uF ceramic capacitors are recommended to reduce the effects of current transients on VOUT.
NC	5	**Not Internally Connected.**
VCNTL	6	**Supply Input for Control Circuit.** This pin provides bias voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the V_{CNTL} . For the device to regulate, the voltage on this pin must be at least 2.0V greater than the output voltage, and no less than V_{CNTL_MIN}. V_{CNTL} input voltage must be ready before V_{IN} input voltage.
NC	7	**Not Internally Connected.**
NC	8	**Not Internally Connected.**
GND	9 (Exposed PAD)	**Ground.** The exposed pad acts the dominant power dissipation path and should be soldered to well design PCB pads as described in the *Application Informations Chapter.*

Function Block Diagram



Absolute Maximum Ratings (Note1)

- Input Voltage V_{IN} ---------- -0.3V to +6V
- Control Voltage V_{CNTL} ---------- -0.3V to +6V
- Reference Input Voltage V_{REFEN} ---------- -0.3V to +6V
- Output Voltage V_{OUT} ---------- -0.3V to +6V
- Power Dissipation, PD@T_A=25℃, PSOP-8----------2.0W
- Thermal Resistance, θ_{JA}, PSOP-8----------50℃/W
- Thermal Resistance, θ_{JC}, PSOP-8----------5℃/W
- Junction Temperature---------- 125°C
- Lead Temperature (Soldering, 10 sec.)---------- 300°C
- Storage Temperature ---------- –65°C to 150°C

Recommended Operating Conditions

- V_{IN} ---------- +1.0V to V_{CNTL}
- V_{CNTL} ---------- +4.5V to +5.5V
- Junction Temperature ---------- -40°C to 125°C
- Ambient Temperature---------- -40°C to 85°C

Electrical Characteristics

V_{CNTL}=5V, V_{IN} = 1.8V, V_{REFEN}, T_A=25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Section						
Control Input Voltage	V_{CNTL}		4.5	--	5.5	V
POR Threshold	V_{PORTH}	V_{CNTL} rising	--	3.6	--	V
POR Hysteresis	$V_{PORTHHYS}$		--	0.2	--	V
Control Operation Current	I_{CNTL}	I_{OUT} = 0A	--	0.7	2.5	mA
Shutdown Current	I_{SD}	V_{REFEN}=0V	--	50	90	uA
Output Voltage						
Output Offset Voltage	V_{OS}	I_{OUT} = 0A	-20		20	mV
Load Regulation	ΔV_{LOAD}	I_{OUT} = ±1A	-20		20	mV
Dropout Voltage	$V_{DROPOUT}$	V_{CNTL}=4.5V, I_{OUT}=1.5A, V_{OUT} = 1.25V		225	525	mV
		V_{CNTL}=4.5V, I_{OUT}=1.0A, V_{OUT} = 1.25V		150	350	mV
Protection						
OCP Threshold Level	I_{OCP}	Source / Sink	2.1	3.0	4.2	A
Output Short Circuit Current	I_{SC}	Source / Sink	--	1.5	--	A
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C

Thermal Shutdown Hysteresis	T_{SDHY}		--	30	--	°C
REFEN Shutdown						
Enable High Level	V_{EN}		0.4	--	--	V
Disable Low Level	V_{SD}		--	--	0.15	V

Typical Characteristics

V_{CNTL}=5V, C_{IN}=10uF, C_{OUT}=10uF, T_J=25℃, unless otherwise specified

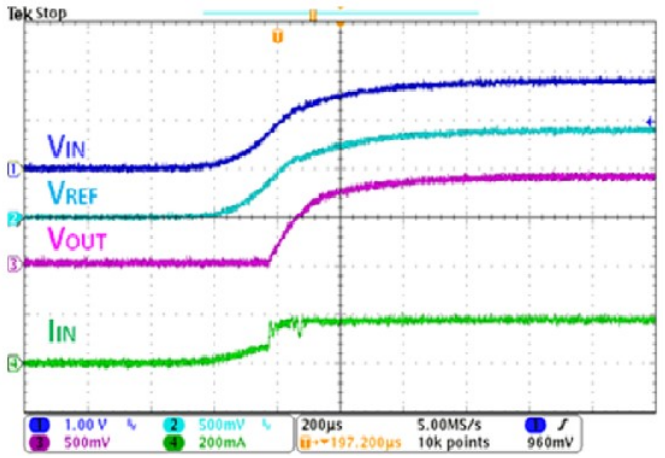


Fig 1. Power ON from V_{IN}

V_{IN}=1.8V ; V_{OUT}=0.9V ; Load=5Ω

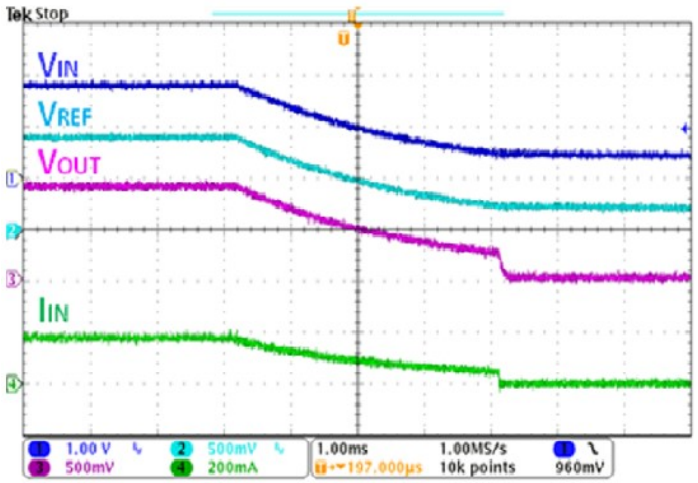


Fig 2. Power OFF from V_{IN}

V_{IN}=1.8V ; V_{OUT}=0.9V ; Load=5Ω

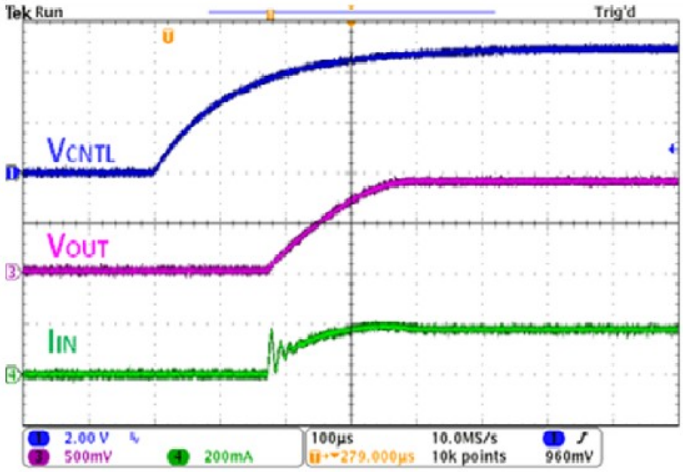


Fig 3. Power ON from V_{CNTL}

V_{IN}=1.8V ; V_{OUT}=0.9V ; Load=5Ω

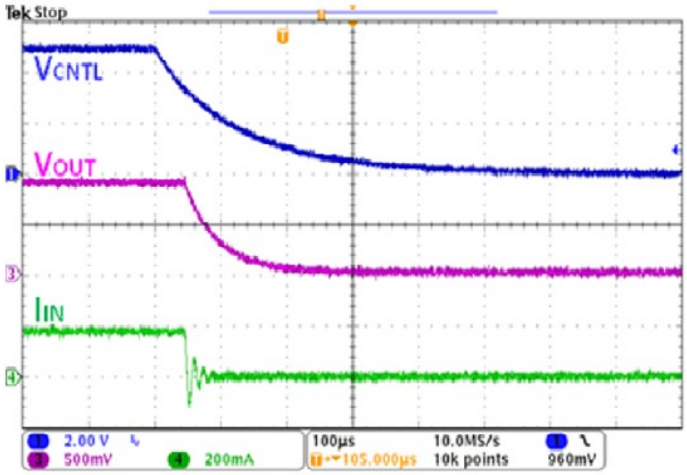


Fig 4. Power OFF from V_{CNTL}

V_{IN}=1.8V ; V_{OUT}=0.9V ; Load=5Ω

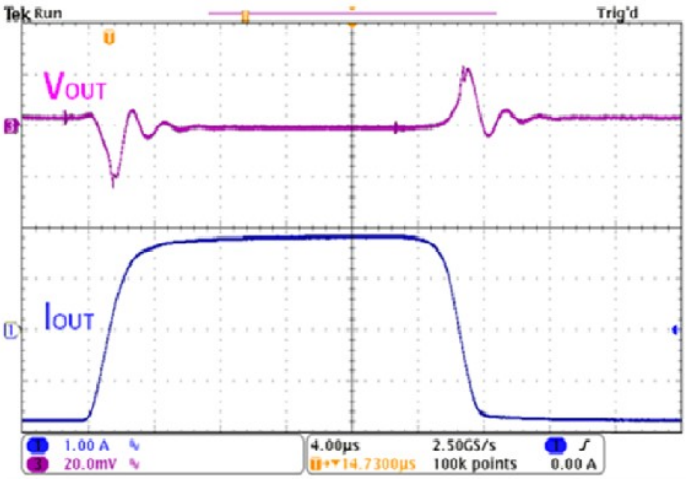


Fig 5. Load Transient Response

V_{IN}=1.8V ; V_{OUT}=0.9V

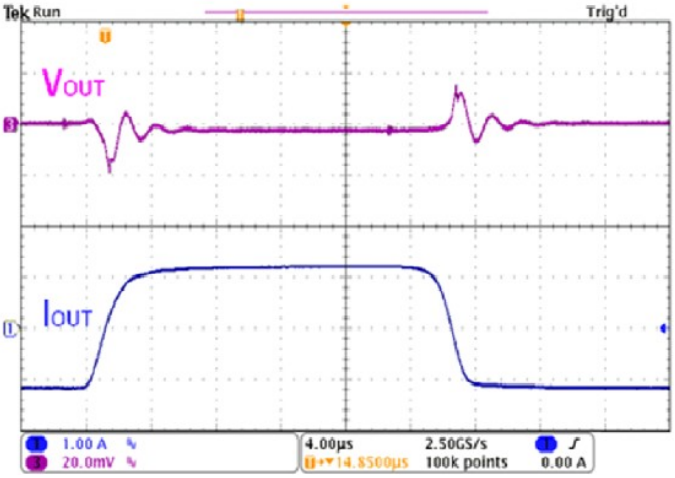


Fig 6. Load Transient Response

V_{IN}=1.2V ; V_{OUT}=0.6V

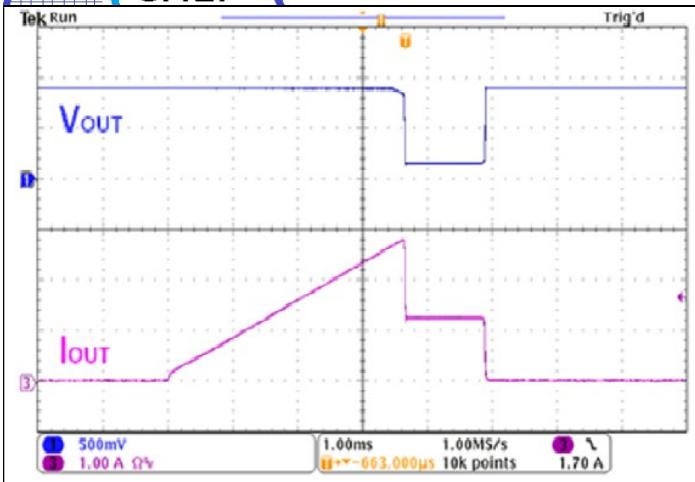


Fig 7. OCP Source
V_{IN}=1.8V ; V_{OUT}=0.9V

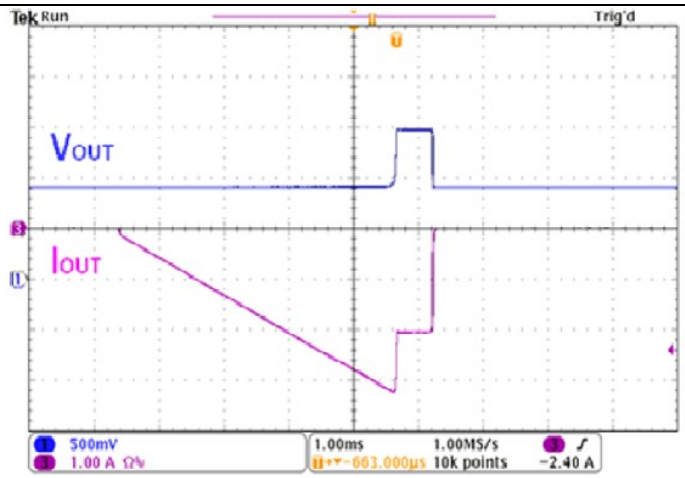


Fig 8. OCP Sink
V_{IN}=1.8V ; V_{OUT}=0.9V

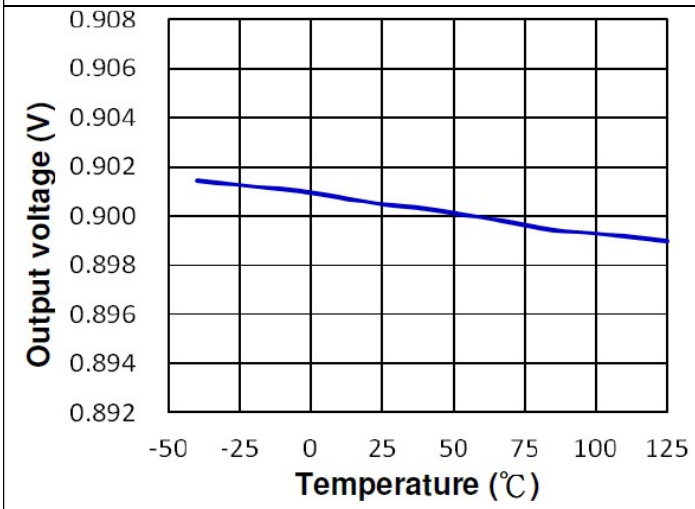


Fig 9. Vout=0.9V vs Temperature

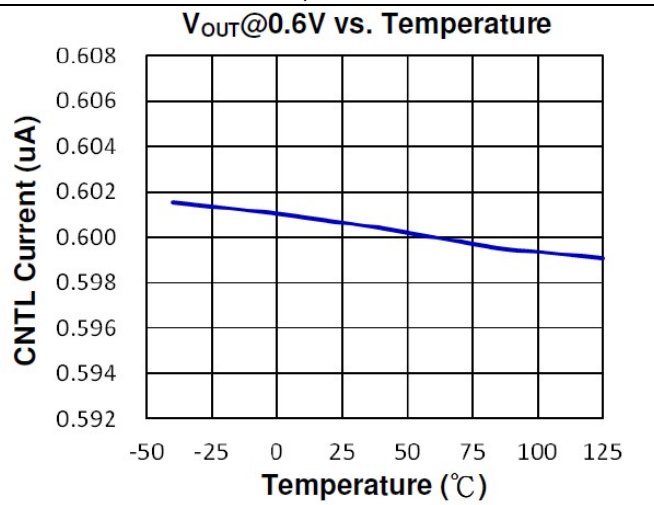


Fig 10. Vout=0.6V vs Temperature

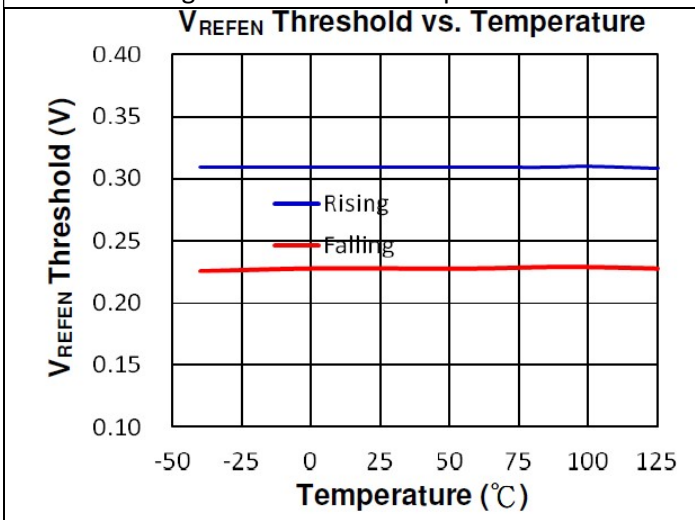


Fig 11. V_{REFEN} Threshold vs Temperature

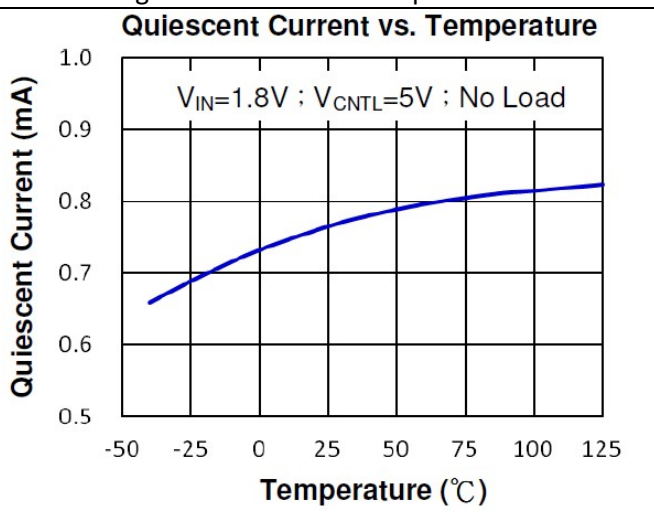


Fig 12. Quiescent Current vs Temperature

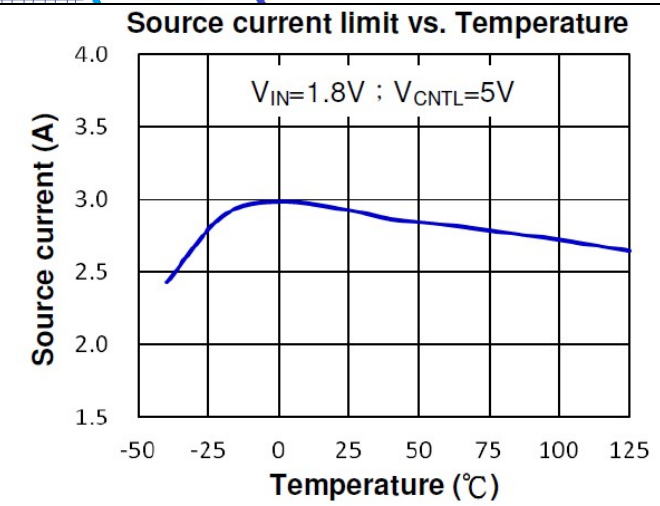


Fig 13. Source Current Limit vs Temperature

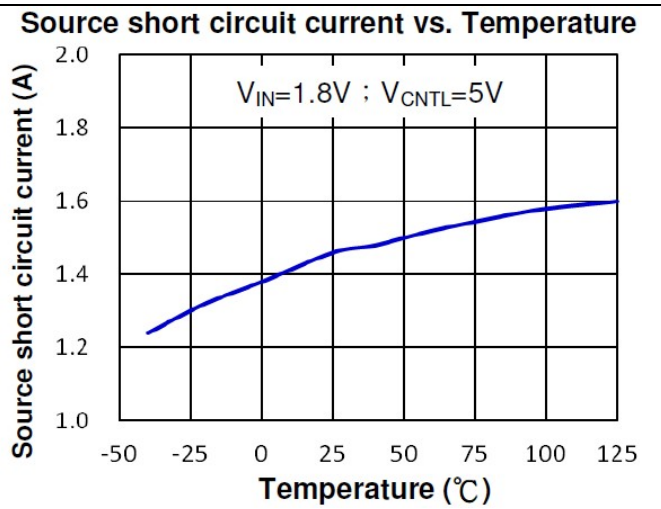


Fig 14. Source short circuit Current vs Temperature

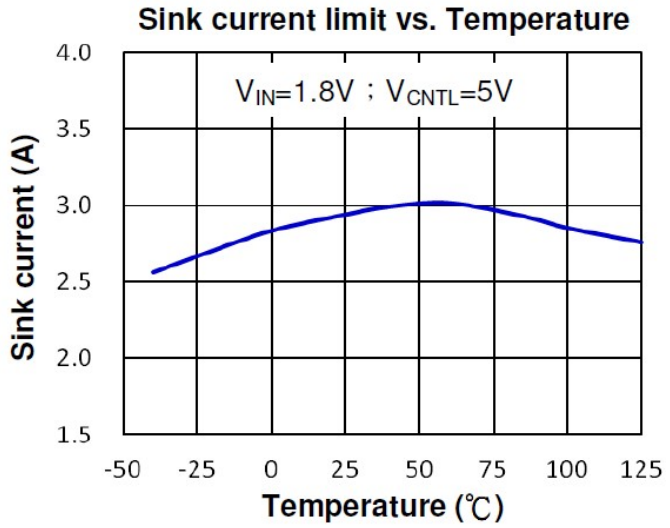


Fig 15. Sink Current Limit vs Temperature

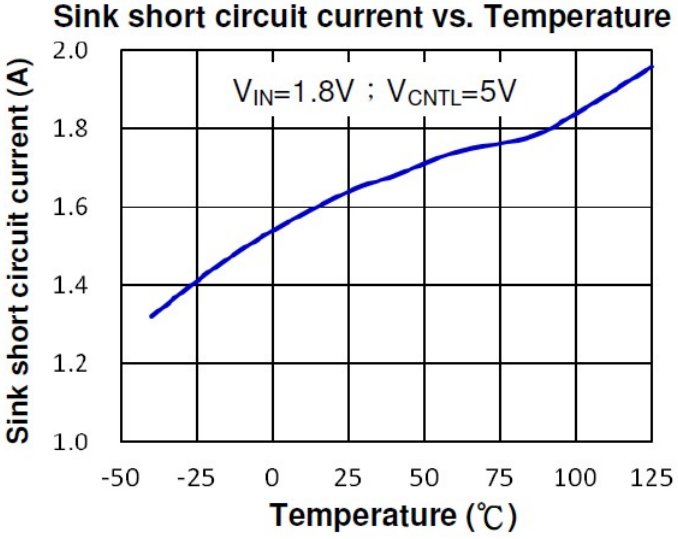


Fig 16. Sink short circuit Current vs Temperature

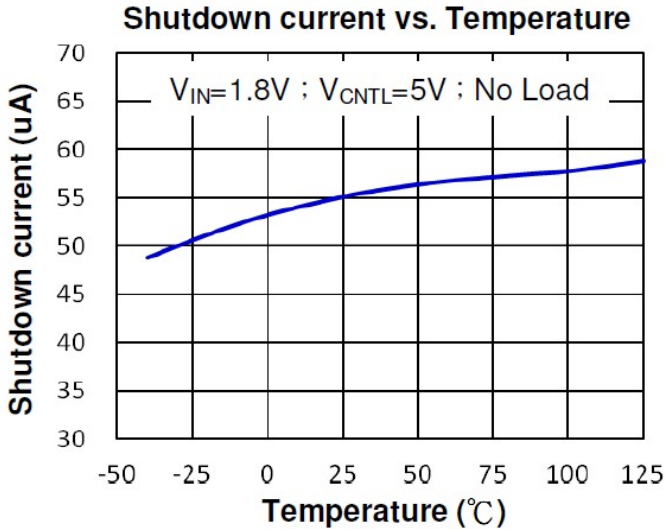


Fig 17. Shutdown Current vs Temperature

IC Operation Information

Basic Operation

The CR2045 is an ultra low dropout linear regulator specifically designed to provide termination voltage for DDR memory system. Designed with low on-resistance NMOSFETs, this device is capable of sinking/sourcing up to 2A output current.

This device works with dual supplies, a control input for the control circuitry and a power input as low as 1.0V for providing current to output. The output voltage is tightly regulated to track reference voltage input within 20mV variation with fast to line/load transient.

Other features include chip shutdown function, soft-start, on-chip thermal protection, and bi-directional current limit protection.

Power On Reset

The CR2045 mainly consists of power on reset and chip enable, pass transistors, current limit, error amplifier and temperature protection as shown in Functional Block Diagram. The CR2045 continuously monitors control input and power input for power on reset (POR) to ensure the device can work properly. The typical POR rising levels are 3.6V and 0.6V for control input and power input respectively.

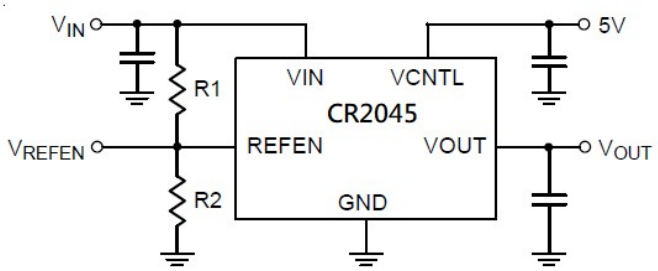
Enable and Shutdown

CR2045 is enabled if the voltage of the REFEN pin is greater than 0.4V. If the voltage of the REFEN pin is less than 0.15V, the IC will be disabled.

Output Voltage Setting

The CR2045 is a high-speed linear regulator designed to generate termination voltage in Double Data Rate (DDR) memory system. Besides, the RT9045 could also serves as a general linear regulator. The CR2045 accepts an external reference voltage at the REFEN pin and provides an output voltage regulated to this reference voltage level as shown in Figure, where

$V_{OUT} = V_{IN} \times R2 / (R1 + R2)$



Soft-Start

The CR2045 builds in an internal soft-start circuit to prevent inrush current during start-up. The internal soft-start time depends on REFEN voltage. For DDRIII application (REFEN = 0.75V), soft-start time is around 100μs..

Over Current Limit Function

CR2045 features over current limiting function as well as output short circuit current fold back function. Typically, before the thermal protection is triggered, CR2045 can limit its output current to 3.0A. When output voltage is decreased, the limiting current level also decreases. When VOUT is short to GND, or VOUT voltage is zero, the output current level is limited to 1.5A, typically.

Input and Output Capacitor Selection

For CNTL pin, a 1uF ceramic capacitor is enough for bypass the supply of CNTL to GND. For VIN pin, 10uF or larger ceramic capacitor is required to provide bypass path in transient current demand. VOUT pin is also recommended to have 10uF or larger ceramic capacitor to be stable and reduce the VOUT voltage dip when fast loading transient is happened.

Thermal Consideration

The CR2045 integrates internal thermal limiting function to protect the device from damage during fault conditions. However, continuously keeping the junction near the thermal shutdown temperature may remain possibility to affect device reliability. It is highly recommended to keep the junction temperature below the recommended operation condition 125℃ for maximum reliability.

Power dissipation in the device is calculated as:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{CNTL} \times I_{CNTL}$

It is adequate to neglect power loss with respective to control circuit V_{CNTL} x I_{CNTL} when considering thermal management in CR2045. Take the following moderate operation condition as an example: V_{IN} = 2.5V, V_{OUT} = 1.5V, I_{OUT} = 1A, the power dissipation is:

$P_D = (2.5V - 1.5V) \times 1A = 1.0W$

This power dissipation is conducted through the package into the ambient environment, and, in the process, the temperature of the die (T_J) rises above ambient. Large power dissipation may cause considerable temperature raise in the regulator in large dropout applications. The geometry of the package and of the printed circuit board (PCB) greatly influence how quickly the heat is transferred to the PCB and away from the chip. The most commonly used thermal metrics for IC packages are thermal resistance from the chip junction to the ambient air surrounding the package (θ_{JA}):

$\theta_{JA} = (T_J - T_A) / P_D$

θ_{JA} specified in the Thermal Information section is measured in the natural convection at T_A = 25℃ on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the exposed pad for PSOP-8 package.

Given power dissipation PD, ambient temperature and thermal resistance θ_{JA}, the junction temperature is calculated as:

$T_J = T_A + \Delta T_{JA} = T_A + P_D \times \theta_{JA}$

To limit the junction temperature within its maximum rating, the allowable maximum power dissipation is calculated as:

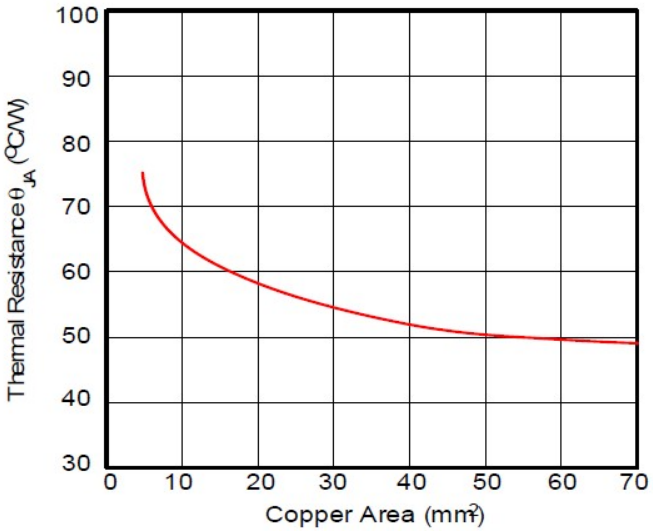
$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125℃, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. θ_{JA} of PSOP-8 packages is 75℃/W on JEDEC 51-7 (4 layers, 2S2P) thermal test board with minimum copper area. The maximum power dissipation at T_A = 25℃ can be calculated as:

$P_{D(MAX)} = (125℃ - 25℃) / 75℃/W = 1.33W$

The thermal resistance θ_{JA} highly depends on the PCB design. Copper plane under the exposed pad is an effective heatsink and is useful for improving thermal conductivity.

Figure shows the relationship between thermal resistance θ_{JA} vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at TA = 25℃. A 50mm^2 copper plane reduces θ_{JA} from 75℃/W to 50℃/W and increases maximum power dissipation from 1.33W to 2W.

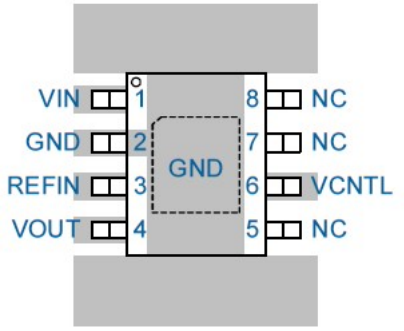


Layout Consideration

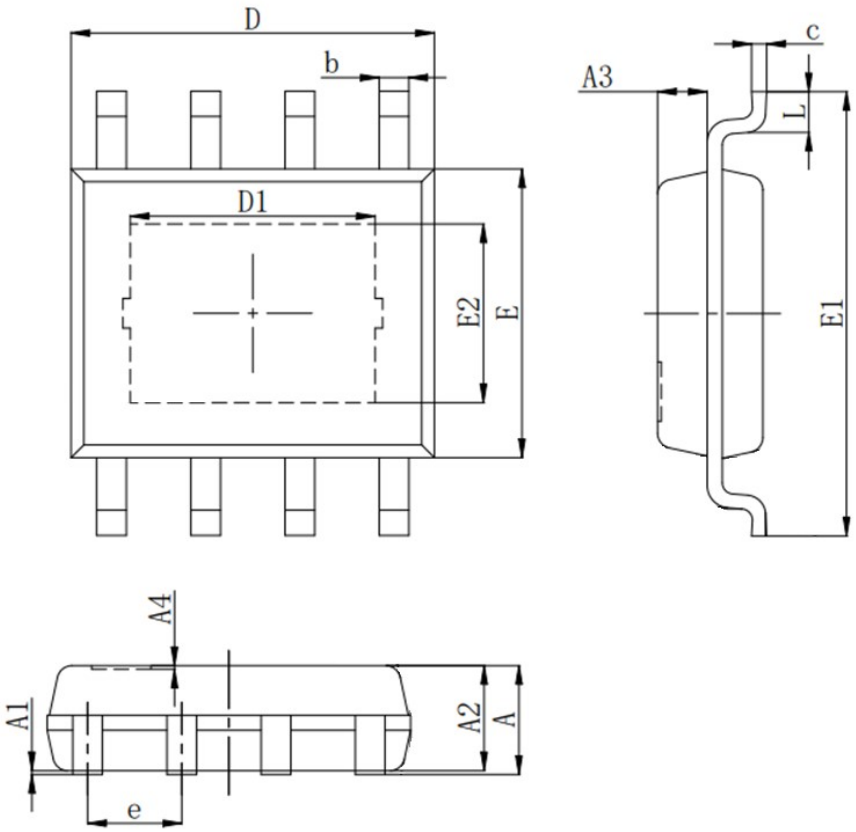
1. Place a local bypass capacitor as closed as possible to the VIN pin. Use short and wide traces to minimize parasitic resistance and inductance.

2. The exposed pad should be soldered on GND plane with maximum area and with multiple vias to inner layer of ground place for improved thermal performance.

3. Connect voltage divider directly to the point where regulation is required. Place voltage divider close to the device.



Package Information
PSOP8



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.30	1.50	1.70
A1	0.00	0.10	0.15
A2	1.35	1.42	1.55
A3	0.645	0.670	0.695
A4	0.02		0.05
c	0.170	0.203	0.250
E	3.8	3.9	4.0
E1	5.80	6.00	6.20
2	2.183	2.283	2.383
L	0.45	0.60	0.75
b	0.33	0.40	0.51
D	4.80	4.90	5.00
D1	3.272	3.372	3.472
e		1.27	